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Scientific Officer
Naval Research Laboratory
Attn: Dr. Geoffrey Summers Code: 6615
4555 Overlook Avenue, SW
Washington, DC 20375-5326

Reference: Quarterly Progress Report for Contract No. N00014-94-C-2030

Dear Sir/Madam:

In accordance with the requirements of the above-referenced contract, I am enclosing Spire's Quarterly Progress Report entitled "InP Solar Cell Development on Inexpensive Silicon Substrates," for 22 Feburary 1994 through 22 May 1994.

Please contact me with any questions or comments you may have regarding this report.

Yours truly,

Spire Corporation

Steven J. Wojtczuk

Steven J. Wojtczuk, Ph.D.
Principal Investigator

Enclosure

cc: R. Little
Contracts (2)
QR-10158.01

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DTIC QUALITY INSPECTED 1

Report Number: QR-10158.01
Report Period: 22 February 1994
through 22 May 1994

CONTRACT TITLE AND NUMBER:

InP Solar Cell Development on Inexpensive Si Substrates
N00014-94-C-2030

CONTRACTING AGENCY:

Naval Research Laboratory
Bldg. 71 Code 6615
4555 Overlook Ave. S.W.
Washington, DC 20375

CONTRACTOR'S NAME AND ADDRESS:

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Bedford, MA 01730-2396

CONTRACT PERIOD: 22 February 1994 to 22 February 1995

STATUS:

Table I shows the current program schedule.

94-26687

Table I *Program schedule.*

Tasks	Feb 94	Mar 94	Apr 94	May 94	Jun 94	Jul 94	Aug 94	Sep 94	Oct 94	Nov 94	Dec 94	Jan 95	Feb 95
1. Optimize Emitter		S	X	X	X	X	X	E	D1				
2. Process Technology							S	E	D2				
3. NRL Small Cells							S/E	D3					
4. Dev. InP/Si Growth		S	X	X	X	X	E	D4					
5. Si Wafer Thickness				S	X	X	X	E	D5				
6. Large Cell Demo									S	X	X	E	D6

Legend: S - Task started
X - Task ongoing
E - Task expected to end
D# - Expected cell delivery

Deliveries: D1 - > 48 1x1 cells, 240 DLTS diodes
D2 - > 6 1x1 cells
D3 - 2 wafers 0.5x0.5 cells, 60 DLTS
D4 - > 20 1x1 cells
D5 - > 18 1x1 cells
D6 - > 100 2x2 cells, > 4 2x4 cells

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Task 1 - Optimize Emitter/Base Dopants - In this section, we describe some of the differences between Spire's previous N-on-P technology and the P-on-N technology being developed for this program. Results of a 17% P/N InP cell, the best made to date are also summarized. The main reason for the change to a P/N cell is that P/N heteroepitaxial InP cells on Si wafers do not have an unintentional back-biased junction at the InP/Si interface that occurs in N/P heteroepitaxial cells. However, the sheet resistance of the emitter of a P/N cell is much higher than an N/P cell:

	Maximum Doping	Typical Mobility	Typical Resistivity
P-InP Emitter:	~2 x 10^{18} cm^3	~100 cm^2/V-s	~0.03 Ω-cm
N-InP Emitter:	~10^{19} cm^3	~200 cm^2/V-s	~0.0003 Ω-cm

For the same emitter thickness, a P/N InP cell has about 100X higher sheet resistance than the N/P cell. In Phase I, Spire attempted to keep the sheet resistance loss of the new P/N cells approximately the same as the 19% N/P cells with 300Å emitters and gridlines on 700 μm center-to-center spacings. This resulted in P/N cells with ~2400Å emitter thicknesses and 250 μm grid spacings. The P/N cells had an 8X thicker emitter, and with the closer gridline spacing had only (250/700) or about ⅓ the photocurrent of the N/P cell flowing to each set of gridlines, so that the closer gridlines reduced the I^2R loss by the square of this, or about 8X. The total I^2R loss expected from the sheet resistance should then be about equal in both P/N and N/P cells. The Phase 1 cells did indeed have fill-factors over 84%, equal to the best N/P cells. However, photocurrents from Phase I P/N cells were only about ⅔ that of Spire's record N/P cells. This was due mainly to the thicker emitter used in the P/N cells. In retrospect, we should not have used the criteria of a similar emitter sheet resistance for the P/N cell as the N/P as a constraint during the P/N cell design, as the following data shows for P/N InP cells made recently with about 500Å emitters, much thinner than used in Phase I. These (Figure 1) cells had better efficiencies, up to 17%, despite somewhat poorer fill factors (less than 80%).

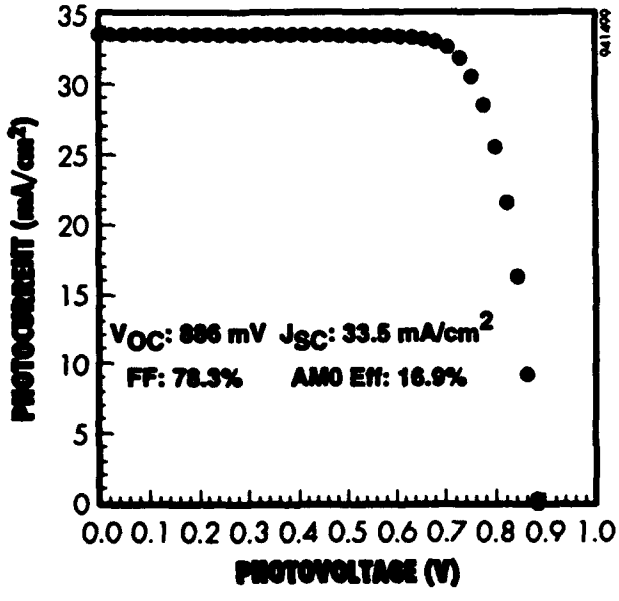

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Figure 1 *Illuminated AM0 I-V curve of a Spire P/N InP cell on InP wafer.*

Figure 2 shows the absolute measured internal and external quantum efficiency, and the reflectance. The AM0 photocurrent obtained by integrating the quantum efficiency against the AM0 spectrum agrees well with the solar-simulator measured photocurrent.

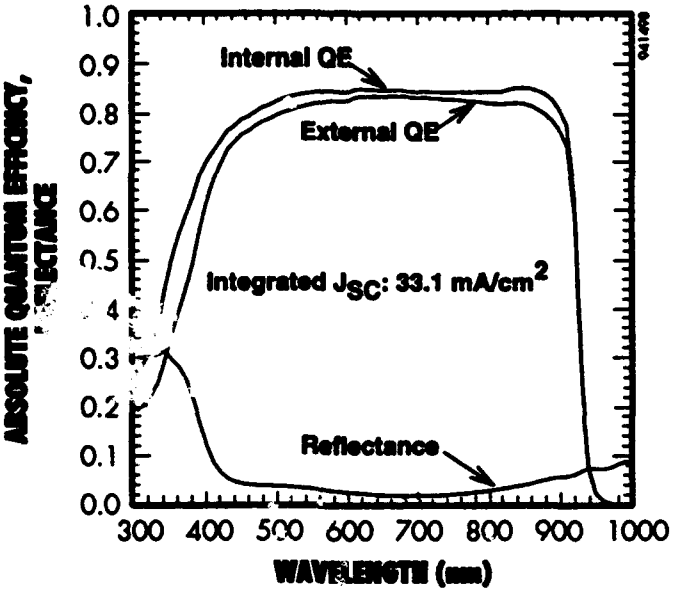

Figure 2 *Measured quantum efficiency of a P/N InP cell on InP (same cell as Figure 1).*

Task 2 - Optimize P/N Cell - This task is scheduled to begin in August 1994.

Task 3 - Produce Quantities of Small Optimized N/P and P/N Cells - This task is scheduled to begin in August 1994.

Task 4 - Optimize the InGaP Grading Layer - Epilayers are being grown by MOCVD using trimethylindium, triethylgallium, and phosphine at 76 torr and a low temperature, 600°C, to limit zinc diffusion and emitter junction depth. Dimethylzinc is being used for all P-type and silane for N-type doping. InP is lattice-mismatched to Si (5.87 vs. 5.43Å, ~8% mismatch). A high density of defects, mainly dislocations, form to accommodate the mismatch. If these defects thread upward into the cell through the junction, they increase the dark current and act as minority carrier recombination sites, lowering cell efficiency. For lattice-mismatched cells, grading layers are used to attempt to bend the threading dislocations harmlessly away parallel to the plane of the cell junction.

$In_xGa_{1-x}As$ grading layers have been used as the interface between N-on-P InP cells on GaAs (National Renewable Energy Laboratory) and Si wafers (Spire). With an $In_xGa_{1-x}As$ grade, one starts with GaAs and must end the grade exactly at $In_{0.53}Ga_{0.47}As$, the composition lattice-matched to InP. If this final composition is off slightly, a whole new set of harmful dislocations may be generated above the grading layer in the cell.

However, with an $In_xGa_{1-x}P$ grading layer, the critical $In_{0.49}Ga_{0.51}P$ composition is the first grown composition at the bottom of the grading layer, where extra dislocations will do comparatively little harm since these dislocations will be influenced by all the thickness of the dislocation-reducing grade itself. The final composition, at the top of the grading layer, is simply InP, "automatically" lattice-matched to the InP cell. The $In_xGa_{1-x}P$ grading layers should be a more manufacturable process since the compositional control requirements are greatly relaxed compared to $In_xGa_{1-x}As$ grading layers.

We are currently examining the question of how best to distribute the strain in the graded layer in order to maximize the dislocation reduction.

Task 5 - Silicon Substrate Thickness - This work during this performance period was aimed at establishing a baseline process for the direct deposition of InP thin films on Si substrates in a single growth run. This developed process is reproducible and production amenable. The tasks conducted to achieve the above objective include: a) establish the deposition parameters for GaAs on three-inch diameter Si substrates in a SPI-MOCVD™ 100S reactor, b) establish the deposition parameters for InP/GaAs/Si in a single growth run, c) deposit InP/GaAs/Si with minimum GaAs buffer layer thickness.

The epitaxial growth of InP-on-Si faces several areas of difficulty, including: 1) lattice mismatch, which leads to a large density of dislocations, 2) thermal expansion mismatch which results wafer bowing and eventual film cracking, and 3) polar-on-nonpolar growth which leads to antiphase domains.

Lattice Mismatch- There is a large lattice mismatch between InP and Si (about 8%) compared to GaAs-on-Si (4%). This leads to the formation of a high density of misfit dislocations at the InP/Si interface. A GaAs buffer can act as a transition zone that will bridge the lattice mismatch and improve the crystalline quality of the InP overlayer.

Thermal Expansion Mismatch - Tensile stress in epitaxial layers caused by thermally mismatched materials can lead to film cracking and wafer bowing during cooling from the growth temperature. This has been a serious problem with the growth of GaAs-on-Si. Cracks have been reported in layers thicker than a few microns; wafer bowing interferes with subsequent lithography. The thermal expansion coefficient of InP (4.5×10^{-6}/°C) is more closely matched to Si (2.3×10^{-6}/°C) than GaAs (6×10^{-6}/°C) is to Si. Therefore, upon cooling from the growth temperature, the InP overlayer is expected to experience less residual tensile stress compared to the GaAs buffer. The tensile stress in the InP film will be a function of the deposition temperature and the GaAs layer thickness.

Polar-on-nonpolar Growth - This condition can lead to the formation of antiphase boundaries (APBs) within the GaAs. To suppress APBs the Si surface should only contain steps that are even numbered in terms of atomic height. This condition is relatively easy to achieve on a surface which is oriented a few degrees off (100). In the present research effort the N^+ Si substrates are oriented 4 to 7 degrees off the (100) towards the [111] direction. This orientation results in reproducible single domain InP/GaAs on Si films with excellent surface morphology.

The conventional approach for InP/GaAs/Si typically involves two separate MOCVD runs in two separate MOCVD reactors, one for the GaAs/Si buffer and one to grow the InP cell. Separate reactors are used since in the past each reactor was dedicated to specific material systems. The GaAs on Si deposition takes 4 to 6 hours and consists of a high temperature bake of the substrate to thermally desorb the native silicon dioxide and provide a clean surface for the deposition of a GaAs nucleation layer at low temperature (400 to 500°C). The substrate temperature is then raised to 600 to 700°C for the deposition of the GaAs buffer layer (1 to 2 μm thick). Typically, once this process is working well, a number of the GaAs/Si substrates are grown and stored. These GaAs/Si wafers were then later used as the "starting" wafers for growth of the InP cell in a different MOCVD reactor than the one used for the GaAs/Si growth. The InP cells are typically 3 to 5 μm thick and take another 4 to 6 hours to grow.

Although the above approach works, it has a number of short comings including: a) high surface defect density due to excessive handling of the substrate through two MOCVD runs; b) excessive wafer bow due to the thick GaAs/Si buffer layer, since GaAs has a high thermal expansion coefficient mismatch with Si (InP and Si are much closer); c) high cost per wafer due to the long time needed to complete two MOCVD runs. Figure 3 shows a flow chart illustrating the advantages of depositing InP/GaAs/Si in a single MOCVD run. The work conducted in the present performance period was aimed at addressing the shortcoming.

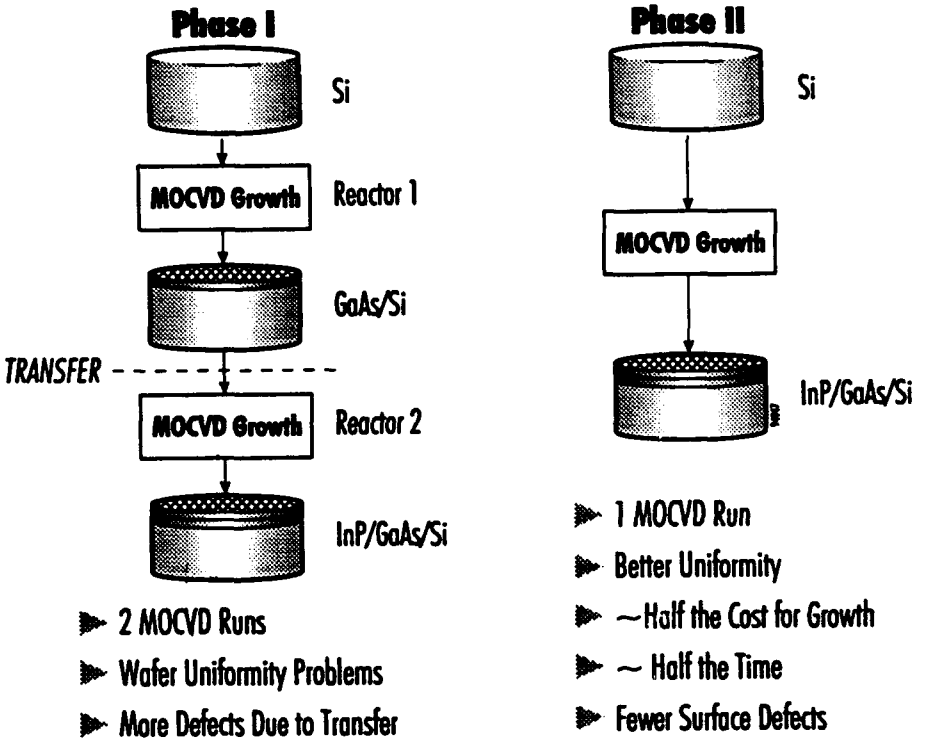

Figure 3 *Process sequence for depositing InP/GaAs/Si in Phase I compared to Phase II.*

a) Establishment of deposition parameters for GaAs on three-inch diameter silicon substrates in a SPI-MOCVD 100S reactor

Spire's baseline process for GaAs on Si was established for a barrel-shaped reaction chamber using trimethylgallium (TMG) and arsine precursors. In order to establish deposition conditions for GaAs/Si that are compatible with InP/InGaAs, a SPI-MOCVD 100S vertical configuration reaction chamber was used and TMG was replaced by triethylgallium (TEG) for precise control of lattice matched In-based ternary compounds. New deposition parameters for GaAs/Si that are compatible with the 100S reaction chamber configuration and the new precursors were developed. Substrate bake-out, and nucleation times and temperatures were the main parameters optimized. Following the high temperature bake-out step, a thin GaAs nucleation film (< 150Å thick) was deposited at 430°C at a low V/III ratio (10 to 20) to achieve maximum surface migration of the Ga-species. Due to the low decomposition temperature of TEG compared to TMG and the relatively high minimum flow imposed by the Arsine mass flow controller, it was difficult to control the GaAs growth rate to reliably deposit the nucleation film. This problem was resolved by reducing the nucleation temperature to 400°C resulting a 30% reduction in the growth rate and hence providing a better control over the growth rate.

The quality of the GaAs/Si films was verified using double crystal X-ray diffractometry and Nomarski optical microscopy on a 1 to 2 μm thick film deposited at convention growth conditions. Figure 4 shows a typical surface morphology for GaAs/Si deposited in SPI-MOCVD 100S reactor. The X-ray line width for a 1 μm thick film is in the range of 500 to 600 arcsec which is typical for as-deposited GaAs/Si films.

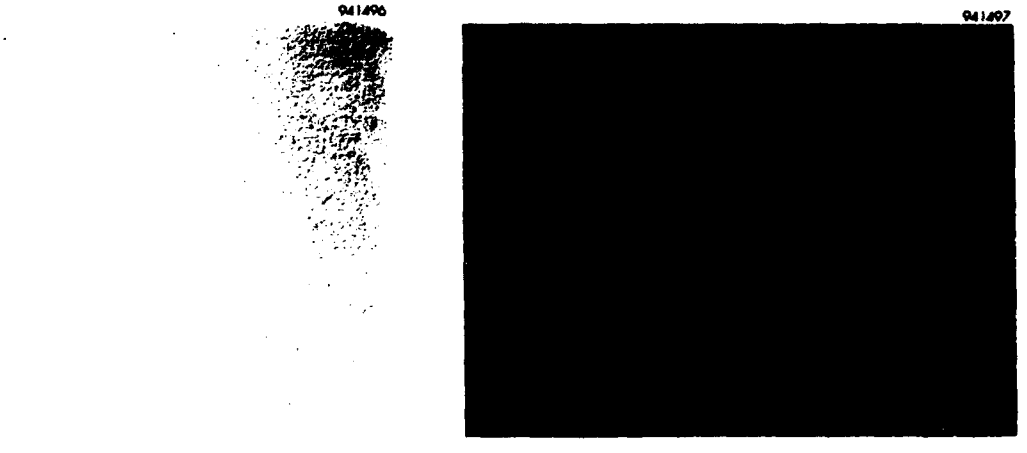

Figure 4 *Nomarski optical micrographs illustrating the surface morphology characteristics for a) GaAs/Si, and b) InP/GaAs/Si each deposited in a single MOCVD run.*

b) Establishment of deposition parameters for InP/GaAs/Si in a single growth run.

The important guidelines for this task were to develop low-temperature deposition of InP/GaAs/Si in a single MOCVD run at relatively low temperatures (600°C). The baseline process was developed using a GaAs buffer layer of 1 μm, a 600°C deposition temperature to prevent any interdiffusion from the P^+ emitter into the N^- base, a V/III ratio of 200, and a growth rate of 3.2 A/s. The deposited films were nominally undoped and had a background carrier concentration of 10^{15} cm^{-3}. The InP/GaAs/Si films had excellent surface morphology and typical X-ray line width of 500 to 600 arcsec for a 1 to 2 μm thick film.

c) Deposition of InP/GaAs/Si with minimum GaAs buffer layer thickness.

Previously, we discussed the effect of the thermal expansion mismatch on wafer bow, which generally increases with thermal mismatch, film thickness, deposition temperature, thinner wafers, and substrate area. We currently use three-inch diameter substrates that are 25 mils thick and plan to go to thinner substrates and eventually four-inch diameter wafers. It is advantageous to minimize the thickness of the GaAs buffer since it has a larger thermal mismatch with Si compared to InP. This has the advantage of not only minimizing wafer bow, but of reducing the deposition time so that the entire InP/Si cell structure could be grown in approximately 4-6 hours, about half the time presently used. We successfully deposited InP/GaAs/Si with GaAs buffer layer thicknesses < 150Å with excellent surface morphology as shown in Figure 5 above.

In addition to the above development work, Si N^{++} substrate wafers of 8, 12, 16, and 20 mil thickness were ordered and received in this time period. We expect to begin growths on various substrate thicknesses in August, 1994. These growths will determine the thinnest wafer feasible for this program. We are cognizant of recent information supplied to us by the Navy that 12 mil wafers would be adequate if growths on 8 mil wafers result in excessive bow due to thermal stress.

Task 6 - Production of Large Optimized Cells - This task is scheduled to begin in October 1994.

Steven J. Wojtczuk
Principal Investigator

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